

Abstract for Submission to NVMTS 2004
Twin MONOS: A Nitride-Based Dual Bit Flash Memory

By Seiki Ogura, Tomoya Saito, Kimihiro Satoh, Yoshitaka Baba,
Nori Ogura, Koji Shimeno, Tomoko Ogura

Halo LSI, Inc. 19075 Tanasbourne Drive, Suite 165, Hillsboro, OR 97124, Contact: togura@halolsi.com

Introduction

Nitride based memory is preferred in space applications due to its high reliability against radiation. Twin MONOS is a CMOS, nitride-based memory technology with the additional properties of (1) dual bit double density for lower cost, (2) high program bandwidth, (3) low power operation, and (4) high performance read.

Twin MONOS Technology Advantages

The Twin MONOS memory cell cross section is shown in Fig. 1. It is distinct from other nitride-based and dual-bit memories in that the charge trap regions are separated under side wall control gates. There is no ONO film underneath the center word gate. [1] The side wall gate are very short, and can be controlled independently to give higher cell current and better controllability.

Simple process: The process is based on CMOS technology. A cell size of $5-7F^2$ can be achieved using only 4-5 extra masks, which is suitable for embedded applications. This array is called the metal bit array and is shown in Fig. 2. Four bits share one bit line contact.

Low power operation: The short channel length of the Twin MONOS sidewall control gate provides low voltage operation. During program, the highest voltage can be as low as 5V, compared to 10-12V in conventional flash devices. Cell current during program can be as low as 20nA.

Fast read: Due to the thin oxide word gate, high cell current, and thin oxide periphery, access times can be very fast. A 16Mb 15ns random access testchip has been measured. [3].

High program bandwidth: CHE injection can be done quickly micro-seconds, at low voltages and low currents, so that high program bandwidths of 25MB/sec and greater are possible.

High density: The diffusion bit array is higher density type of Twin MONOS memory array. This is a contactless memory array, and cell sizes of $2.5F^2$ can be achieved with a slightly more difficult process than the metal bit array.

Cycling reliability and high temperature: Because the side wall channel length is only tens of nanometers, the charge trap region can easily covered by both the holes and the electrons for better cycling reliability. Conventional planar devices suffer from mismatch of hole and electron coverage, because hole mobility is lower. [2] Also, less oxide damage occurs because the program/erase voltages are lower. ONO material is very strong to high temperature operation.

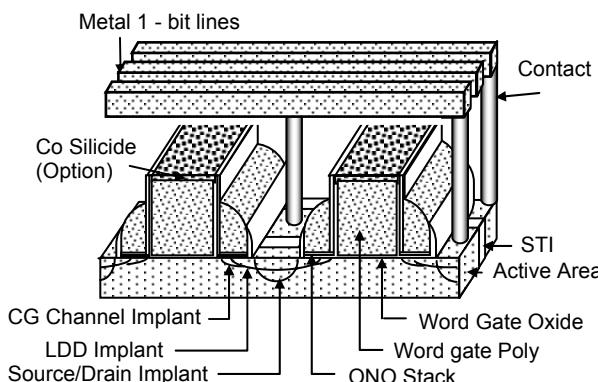


Fig. 1: Twin MONOS cells cross-section.

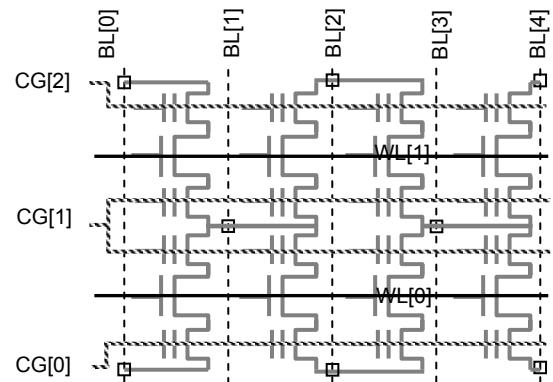


Fig. 4: Schematic representation of metal bit array.

References

- [1] Y. Hayashi, et. al, "Twin MONOS cell with dual control gates", VLSI Technology Symposium, 2000.
- [2] B. Eitan, et. al., NVSM Workshop 2003.
- [3] T. Ogura, et. al., "Embeddable Twin MONOS Flash Memories with 4ns and 15ns Access Times", VLSI Circuits Symposium, 2003.